WHAT IS CLAIMED IS:

1. An apparatus comprising:

a first storage location configured to store a first indication, the first storage location addressable by a first instruction defined by a processor architecture;

a second storage location configured to store a second indication, the second storage location addressable by a second instruction defined by the processor architecture, the second instruction being different from the first instruction;

a third storage location configured to store a mode indication, the mode indication indicative of whether or not a first mode defined in the processor architecture is active; and

a processor configured to generate the mode indication responsive to the first indication and the second indication.

2. The apparatus as recited in claim 1 wherein the first indication is an enable indication defined in the processor architecture to indicate whether or not the first mode is to be enabled.

3. The apparatus as recited in claim 2 wherein the second indication is a paging indication defined in the processor architecture to indicate of whether or not paging is enabled.

4. The apparatus as recited in claim 3 wherein the mode indication indicates that the first

mode is active if the enable indication is in an enabled state and the paging indication indicates that paging is enabled.

5. The apparatus as recited in claim 3 wherein the processor is configured to check a status of one or more indications including the enable indication and the paging indication when changing one of the one or more indications to ensure that the change is permitted by the processor architecture.

6. The apparatus as recited in claim 5 wherein the processor is configured to signal an exception prior to changing the one of the one or more indications if the change is not permitted.

7. The apparatus as recited in claim 5 wherein, if the enable indication is changed from a disabled state to an enabled state, the processor checks that the paging indication indicates that paging is disabled for the change to be permitted.

8. The apparatus as recited in claim 5 wherein, if the enable indication is changed from an enabled state to a disabled state, the processor checks that the paging indication indicates that paging is disabled for the change to be permitted.

9. The apparatus as recited in claim 5 wherein, if the paging indication is changed from indicating that paging is disabled to indicating that paging is enabled, the change is not permitted if the enable indication is in an enabled state and another indication indicates that physical address extension is disabled.

10. The apparatus as recited in claim 5 wherein the one of the one or more indications is an indication of whether or not physical address extension is enabled, and wherein the change is not permitted if the enable indication is in an enabled state.

11. The apparatus as recited in claim 1 further comprising a fourth storage location configured to store a segment selector identifying a segment descriptor including a first operating mode indication and a second operating mode indication, and wherein the processor is configured to generate an operating mode responsive to the mode indication, the first operating mode indication, and the second operating mode indication.

12. The apparatus as recited in claim 1 wherein the first storage location is located within a first register defined by the processor architecture, and wherein the second storage location is located within a second register defined by the processor architecture.

13. The apparatus as recited in claim 12 wherein the third storage location is located within the first register.

14. The apparatus as recited in claim 12 wherein the first register and the second register are incorporated within the processor.

15. The apparatus as recited in claim 14 further comprising a circuit coupled to the first register and the second register, wherein the circuit is configured to generate the mode indication for storage in the third storage location.

16. The apparatus as recited in claim 1 wherein the processor implements the processor architecture.

17. The apparatus as recited in claim 1 wherein the processor emulates the processor architecture.

18. The apparatus as recited in claim 17 wherein the processor executes interpreter software for interpreting instructions defined in the processor architecture.

19. The apparatus as recited in claim 17 wherein the processor executes translator software for translating instructions defined in the processor architecture to instructions executable by the processor.

20. The apparatus as recited in claim 17 wherein the processor executes a combination of: (i) interpreter software for interpreting instructions defined in the processor architecture; and (ii) translator software for translating instructions defined in the processor architecture to instructions executable by the processor.

21. A processor comprising:

a first register configured to store a first indication, the first register addressable by a first instruction;

a second register configured to store a second indication, the second register addressable by a second instruction different from the first instruction; and

a circuit coupled to the first register and the second register, wherein the circuit is configured to generate a mode indication responsive to the first indication and the second indication, wherein the mode indication is indicative of whether or not a first mode defined in a processor architecture of the processor is active, and wherein the circuit is configured to store the mode indication in a location addressable by an instruction.

22. The processor as recited in claim 21 wherein the first indication is an enable indication defined in the processor architecture to indicate whether or not the first mode is to be enabled.

23. The processor as recited in claim 22 wherein the second indication is a paging

indication defined in the processor architecture to indicate of whether or not paging is enabled.

24. The processor as recited in claim 23 wherein the mode indication indicates that the first mode is active if the enable indication is in an enabled state and the paging indication indicates that paging is enabled.

25. The processor as recited in claim 23 wherein the processor is configured to check a status of one or more indications including the enable indication and the paging indication when changing one of the one or more indications to ensure that the change is permitted by the processor architecture.

26. The processor as recited in claim 25 wherein the processor is configured to signal an exception prior to changing the one of the one or more indications if the change is not permitted.

27. The processor as recited in claim 25 wherein, if the enable indication is changed from a disabled state to an enabled state, the processor checks that the paging indication indicates that paging is disabled for the change to be permitted.

28. The processor as recited in claim 25 wherein, if the enable indication is changed from an enabled state to a disabled state, the processor checks that the paging indication indicates that paging is disabled for the change to be permitted.

29. The processor as recited in claim 25 wherein, if the paging indication is changed from indicating that paging is disabled to indicating that paging is enabled, the change is not permitted if the enable indication is in an enabled state and another indication indicates that physical address extension is disabled.

30. The processor as recited in claim 25 wherein the one of the one or more indications is an indication of whether or not physical address extension is enabled, and wherein the change is not permitted if the enable indication is in an enabled state.

31. The processor as recited in claim 21 further comprising a segment register configured to store a segment selector identifying a segment descriptor including a first operating mode indication and a second operating mode indication, and wherein the circuit is configured to generate an operating mode responsive to the mode indication, the first operating mode indication, and the second operating mode indication.

32. The processor as recited in claim 21 wherein the mode indication is also stored in the first register.

33. A method comprising:

storing a first indication in a first storage location addressable by a first instruction;

storing a second indication in a second storage location addressable by a second instruction;

generating a mode indication indicative of whether or not a first mode defined in a processor architecture is active, the generating responsive to the first indication and the second indication; and

storing the mode indication in a third addressable storage location.

34. The method as recited in claim 33 wherein the first indication is an enable indication defined in the processor architecture to indicate whether or not the first mode is to be

enabled.

35. The method as recited in claim 34 wherein the second indication is a paging indication defined in the processor architecture to indicate of whether or not paging is enabled.

36. The method as recited in claim 35 wherein the generating comprises generating the mode indication to indicate that the first mode is active if the enable indication is in an enabled state and the paging indication indicates that paging is enabled.

37. The method as recited in claim 35 further comprising checking a status of one or more indications including the enable indication and the paging indication when changing one of the one or more indications to ensure that the change is permitted by the processor architecture.

38. The method as recited in claim 37 further comprising signalling an exception prior to changing the one of the one or more indications if the change is not permitted.

39. The method as recited in claim 37 wherein the checking comprises, if the enable indication is changed from a disabled state to an enabled state, checking that the paging indication indicates that paging is disabled for the change to be permitted.

40. The method as recited in claim 37 wherein the checking comprises, if the enable indication is changed from an enabled state to a disabled state, checking that the paging indication indicates that paging is disabled for the change to be permitted.

41. The method as recited in claim 37 wherein, if the paging indication is changed from indicating that paging is disabled to indicating that paging is enabled, the change is not permitted if the enable indication is in an enabled state and another indication indicates

that physical address extension is disabled.

42. The method as recited in claim 37 wherein the one of the one or more indications is an indication of whether or not physical address extension is enabled, and wherein the change is not permitted if the enable indication is in an enabled state.

43. The method as recited in claim 33 further comprising generating an operating mode responsive to the mode indication, a first operating mode indication, and a second operating mode indication, wherein the first operating mode indication and the second operating mode indication are included in a segment descriptor identified by a segment selector stored in a fourth storage location.

44. A carrier medium carrying a set of instructions for activating a first mode in a processor, the set of instructions including:

a first one or more instructions to update a first indication to indicate that physical address extension is enabled;

a second one or more instructions to update a page table base register to point to a set of page tables;

a third one or more instructions to update an enable indication to an enabled state; and

a fourth one or more instructions to update a paging indication to indicate that paging is enabled.

45. The carrier medium as recited in claim 44 wherein an order of the first one or more instructions, the second one or more instructions, and the third one or more instructions in

the set of instructions is arbitrary.

46. The carrier medium as recited in claim 44 wherein the fourth one or more instructions are ordered subsequent to the first one or more instructions, the second one or more instructions, and the third one or more instructions in the set of instructions.

47. The carrier medium as recited in claim 44 wherein the set of instructions further includes a fifth one or more instructions to update the paging indication to indicate that paging is disabled, the fifth one or more instructions ordered prior to the first one or more instructions, the second one or more instructions, the third one or more instructions, and the fourth one or more instructions in the set of instructions.

48. A carrier medium carrying a set of instructions for deactivating a first mode in a processor, the set of instructions including:

a first one or more instructions to update a paging indication to indicate that paging is disabled;

a second one or more instructions to update a page table base register to point to a set of page tables; and

a third one or more instructions to update an enable indication to a disabled state.

49. The carrier medium as recited in claim 48 wherein the set of instructions further includes a fourth one or more instructions to update the paging indication to indicate that paging is enabled.